REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested. This is a response to the outstanding non-final Office Action, which was mailed on September 16, 2009.

In a semiconductor storage apparatus according to both of the independent claims, i.e., claims 1 and 16, the featured status polling was further defined to show that it clearly distinguishes from the "signal BUSY" in Nishi, which is the primary reference applied in the outstanding rejection. This will be more clearly understood in the discussion which follows.

Independent claims 1 and 16 set forth a semiconductor storage apparatus to be coupled with a system bus, such as is illustrated with regard to the example embodiment in Fig. 1 of the drawings, although not limited thereto. The flash memory chips 4 in Fig. 1 are illustrative of the featured plurality of nonvolatile semiconductor memories. Each of the nonvolatile semiconductor memories 4 is configured to store sectors of data therein (e.g., each sector including 512 bytes) such as discussed on page 15, line 5, *et. seq.* of the specification (or paragraph [0034] in corresponding publication US 2004/0167653 A1) . As to the control module, an example of which is illustrated with regard to processor 2 and address controller 31 in Fig. 1, is coupled with the system bus (STD BUS 1) and the nonvolatile semiconductor memories 4.

Independent claims 1 and 16 are particularly directed to the aspect of the erasing operation of the nonvolatile semiconductor memories, such as described on page 16, line 12, to page 19, line 6, of the specification (or par. [0036]-[0038] in corresponding publication) in conjunction with the example Fig. 1 embodiment and the relating flow chart in Fig. 4 of the drawings, which concerns the erase operation

according to the invention. Regarding the set forth "control module refers to a table for selecting a first one of said nonvolatile semiconductor memories and sends a first erase command to said first one of said nonvolatile semiconductor memories to initiate a first internal erase operation of data within said first one of said nonvolatile semiconductor memories," related discussion is given on page 17, line 10, *et. seq.* (or par. [0037] in corresponding publication), and Fig. 3 of the specification relates thereto. For example, after having set the sectors-to-be erased in the write management table, the processor 2 sends erase commands into the respective chips of the nonvolatile memories (e.g., flash memories 4) listed in the write management table while updating the designation of the flash memory chip in the table. In accordance with the invention, a second internal erase operation of data is initiated, by a second erase command from the control module, in a second, different one of the plurality of nonvolatile semiconductor memories while the first one of the nonvolatile semiconductor memories is still performing the corresponding first internal erase operation in response to the first erase command.

The invention further calls for, among the featured aspects thereof, the control module to execute status polling in connection with each of the nonvolatile semiconductor memories performing the erase operation. In this regard, independent claim 1, as well as independent claim 16, set forth the following:

> wherein said control module executes status polling from the first nonvolatile semiconductor memory to which said first erase command has been sent and is followed by executing status polling from the second nonvolatile semiconductor memory to which said second erase command has been sent, wherein the status polling is executed by the control module signaling a respective one of the nonvolatile semiconductor memories and receiving a return signal from the respective one of the nonvolatile semiconductor memories, the return signal from the respective one of the nonvolatile semiconductor memories indicates whether the internal erase operation has been

completed within the respective one of the nonvolatile semiconductor memories.

With regard to the example embodiment in Fig. 1 of the drawings, although not to be construed as being limited thereto, and the erase procedure in Fig. 4, the processor 2 further executes status polling in connection with each of the respective memory chips into which the erase command has been initially written in connection with determining if an erase operation within each respectively designated nonvolatile semiconductor memory has been completed. In accordance with the invention, status polling is executed by the control module signaling a respective one of the nonvolatile semiconductor memories and receiving a return signal from that same nonvolatile semiconductor memory, the return signal indicating whether the internal erase operation within the respective nonvolatile semiconductor memory has been completed. In accordance with the invention, the control module executes status polling from the first semiconductor memory into which the first erase command has been sent and is followed by executing status polling from the second nonvolatile semiconductor memory into which the second erase command has been sent (see Fig. 1 in conjunction with the erase procedure in Fig. 4 of the drawings).

It is submitted, the invention according to independent claim 1 and the dependent claims thereof as well as according to independent claim 16 and the dependent claims thereof, as now amended, could not have been achievable from the combined teachings of Nishi (USP 5,724,544) and Robinson et al (USP 5,388,248), and as alleged in the outstanding rejection. Therefore, insofar as presently applicable, the rejection is traversed and withdrawal of the same is respectfully requested.

Nishi discloses an IC memory card for storing picture data. In the featured memory card 1 in Nishi, two nonvolatile memories are provided, one of which is a flash/block erasable-type nonvolatile memory (e.g., FLASHING EEPROM 40) for storing a large amount of data (e.g., picture data), and a second nonvolatile memory, for example, a byte-by-byte erasable EEPROM which is configured for storing supervisory-type data. (Column 2, lines 40-48, in Nishi.) According to Nishi, such a structured memory card provides advantages over a flash-only card in which volume data (e.g., picture data) are stored together with the supervisory data, in that changes to the supervisory data cause needless erasing of the volume data. (Column 1, line 48, to column 2, line 12, in Nishi.)

It is alleged in the rejection that the "signal BUSY" of Nishi's schemed IC memory card 1 relates to status polling according to the present invention. In this regard, the Examiner states the following:

> "...the BUSY signal of Nishi represents the polling operation as claimed."

Applicants, however, respectfully disagree with this assertion. The "signal BUSY" according to Nishi is a signal in which the system controller 22 provides <u>to the host processor</u> to report that processing is underway in the memory card 1, and this BUSY signal, according to Nishi, is <u>not</u> a signal from the individual memories to determine if the internal erasing operation has been completed. It is submitted, there is neither a teaching nor a suggestion in Nishi of the featured status polling between the controller and the respective memories according to that set forth in each of the independent claims 1 and 16 and, correspondingly, in the dependent claims thereof. According to Nishi's IC memory card construction, controller 212 controls the various blocks 202-210 and <u>sends the BUSY signal back to the host processor to report that</u>

processing is underway in the memory card. (Column 4, lines 32-37, in Nishi.) The BUSY signal used in Nishi's system does not constitute status polling in the same sense as that according to the present invention, but rather serves to prevent the host processor from sending data to the memory card. (Column 5, lines 38-46; column 6, lines 15-21, etc., in Nishi.) It is submitted, therefore, status polling as is currently defined in the respective independent claims 1 and 16 was neither taught nor suggested from Nishi.

It is also admitted in the rejection that "Nishi does not teach initiating the second erase command while the first erase operation is still being performed in the first nonvolatile memory." Robinson et al, however, was cited as allegedly "[disclosing] performing simultaneous write and erase operations.... It would have been obvious...to modify the system of Nishi to perform the erase operations in parallel as done by Robinson...". In this regard, it is observed that Robinson does not appear to give any teaching or suggestion concerning the implementing of such parallel erasing operation control. The particularly cited portions of Robinson et al, i.e., column 23, lines 48-55, and column 24, lines 63-68, do not illustrate or teach how to effect an erasing operation control as that according to claims 1+ and 16+ of the present application. It is submitted, therefore, for at least the above reasons, the invention according to independent claims 1 and 16 and also according to the dependent claims thereof could not have been achieved even in view of the combined teachings of Nishi and Robinson et al, and as alleged in the outstanding rejection. Concerning the dependent claims, Applicants consider them to be allowable at least for the same and similar reasons as that rendering independent claims 1 and 16 allowable.
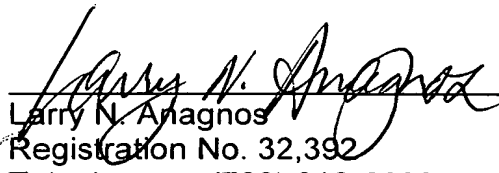
Therefore, in view of the above-made amendments together with the accompanying Remarks, withdrawal of the outstanding rejection, as well as favorable action on pending claims 1-16 and 18-21, together with an early formal notification of allowance of the above-identified application, is respectfully requested.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, he/she is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Docket No. 1487.32253CC8), and please credit any excess fees to such deposit account.

Respectfully submitted,

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